AMENDMENTS TO THE CLAIMS

This listing of claim will replace all prior versions and listings of claim in the application.

1. (currently amended) A method for reading a non-volatile memory arranged in columns and rows, comprising the steps of:

selecting a word-line WLn to be read;

reading an adjacent word line (WLn+1) written after word line WLn;

determining whether the adjacent word line has a threshold voltage greater than a check voltage; and

if the data state of the adjacent word line is above [a] the check voltage, reading a selected bit in word line WLn by selectively adjusting at least [one read parameter] a pre-charge voltage.

2. (currently amended) The method of claim 1 wherein the step of reading a selected bit in word line WLn further includes adjusting [the read parameter is the] a sense voltage.

3. (currently amended) The method of claim 2 wherein the step of reading the selected bit includes increasing the sense voltage.

4. (original) The method of claim 3 wherein the step of increasing the sense voltage includes increasing the sense voltage by an amount equal to a fraction of the maximum coupling effect of the adjacent bit on the selected bit.

5. (original) The method of claim 4 wherein the fraction is one-half.

6. (cancelled)

7. (currently amended) The method of claim [6] 1 wherein the step of reading the bit includes decreasing the pre-charge voltage.

8. (currently amended) The method of claim 7 wherein the step of decreasing the pre-charge voltage includes decreasing the [sense] pre-charge voltage by an amount equal to a fraction of the maximum coupling effect of the adjacent bit on the selected bit.

9. (cancelled)

10. (cancelled)

11. (currently amended) The method of claim 1[0] wherein the check voltage is one half of the voltage threshold distribution.

12. (original) The method of claim 1 wherein the bits hold a multi-state memory, the step of reading an adjacent word line includes determining the threshold voltage state of the bit.

13. (currently amended) The method of claim 12 wherein the step of reading an adjacent word line includes reading the bit at least three times.

14. (currently amended) The method of claim 13 wherein the step of reading the selected bit in the word line further includes decreasing [the]a sense voltage by an amount equal to [the] a coupling effect of the adjacent bit on the selected bit.

15. (currently amended) The method of claim 13 wherein the step of reading the selected bit includes increasing [the] a pre-charge voltage by an amount equal to [the] a coupling effect of the adjacent bit on the selected bit.

16. (cancelled)

17. (currently amended) A method for reading non-volatile memory arranged in columns and rows, comprising the steps of:

determining a selected bit to be read in a first word-line;

reading an adjacent word line written after the first word line;

determining whether a bit adjacent to the selected bit has a threshold voltage greater than a check voltage; and

if the adjacent bit has a threshold voltage greater than the check [value] voltage, reading the selected bit in said first word line by selectively adjusting at least [one read parameter] a pre-charge voltage.

18. (currently amended) The method of claim 17 wherein the step of reading a selected bit in the first word line further includes adjusting [the read parameter is the] a sense voltage.

19. (previously presented) The method of claim 18 wherein the step of reading the selected bit includes increasing the sense voltage.

20. (original) The method of claim 19 wherein the step of increasing the sense voltage includes increasing the sense voltage by an amount equal to one-half of the maximum coupling effect of the adjacent bit on the selected bit.

21. (cancelled)

22. (currently amended) The method of claim [21] 20 wherein the step of reading the selected bit in the first word line includes decreasing the pre-charge voltage.

23. (original) The method of claim 22 wherein the step of decreasing the pre-charge voltage includes decreasing the sense voltage by an amount equal to one-half of the maximum coupling effect of the adjacent bit on the selected bit.

24. (original) The method of claim 17 wherein the check voltage is one half of the voltage threshold distribution of a multi-state cell array.

25. (currently amended) A memory system including code enabling reading data from the system, comprising:

an array of multi-state memory cells arranged in rows and columns;

a controller coupled to the array executing said code, the code performing the steps of:

determining a selected bit to be read in a first row-line;

reading an adjacent row line written after the first row line;

determining whether a bit adjacent to the selected bit has a threshold voltage greater than a check voltage; and

if the adjacent bit has a threshold voltage greater than the check [value] voltage, reading the selected bit in the first row line by selectively adjusting at least [one read parameter] a pre-charge voltage.

26. (currently amended) The system of claim 25 wherein selected bit in the first row line further includes adjusting [the read parameter is the] a sense voltage.

27. (previously presented) The system of claim 26 wherein the step of reading the selected bit includes increasing the sense voltage.

28. (cancelled)

29. (currently amended) The system of claim 2[8]5 wherein the step of reading the selected bit includes decreasing the pre-charge voltage.

30. (previously presented) The system of claim 25 wherein the step of reading the selected bit includes adjusting both a pre-charge voltage and a sense voltage.

31. (currently amended) The system of claim 25 wherein the check voltage is one half of a ~~the~~ voltage threshold distribution of [a] the multi-state cell array.

32. (cancelled)